A 40nm, High Bandwidth, VCO-based Burst-Mode Receiver Backend for EHF Multi-Carrier Wireless

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***Abstract*— A receiver back-end in 40 nm CMOS for an EHF wireless multi-carrier applications is presented. The system is designed to reduce the bandwidth of a multi-tone I/Q decomposed wideband signal after which it is digitized and stored. The bandwidth reduction is applied by means of a reconfigurable sub-sampling operation. The integrated ADCs, performing the digitization, are a time-based dual 128-phase VCO topology implementation. On-chip data buffering of 96 kB is foreseen, capable of storing burst signals of a duration up to 8 μs. The IC is capable to process discrete spectra up to an RF bandwidth of 6 GHz originating from a downconverted 60 GHz signal. A measured effective resolution of 6 bits is realized thanks to the inherent first order noise shaping of the built-in ADC. The SFDR is measured at 40 dB. Power consumption for the complete I/Q core, sampling at 3 GHz, is measured to be 106 mW. The area of the 40 nm core is 0.162 mm^2.**

I. Introduction

Recently, certain sub-bands of the extremely-high-frequency (EHF) band (30 — 300 GHz) are opened to custom wireless application development. The 60 GHz band, for example, provides a bandwidth of about 6 GHz world-widely open for new applications [1]. Recent CMOS technology makes implementations of wideband RF-building blocks on this carrier frequency technically feasible. However, baseband analog electronics, processing the down converted signals in receivers, suffer from limited bandwidths. This paper presents a SoC-approach for selective digitization of discrete spectra for wideband multi-carrier positioning and communications applications covering an RF bandwidth of 6 GHz [2]. The discrete, sparse, frequency domain allocation leaves interesting degrees of freedom for design of the digitization approach, from which AC-coupling and bandwidth reduction, solving the baseband bandwidth problem, are the most important ones.

Because of the low supply voltages in today's recent CMOS technologies data converter designs shift to time-based topologies. Consequently, the ADC, as part of the system is based on a time-based, open loop, voltage-controlled oscillator (VCO) structure [3]–[7]. Due to down scaling of the CMOS feature size, ring VCOs achieve high frequencies, even when supply voltages tend to go below 1 V. Additionally, the shaping property of its quantization noise to high frequencies makes this topology an ideal choice.

The paper is organized as follows. Section II provides the high level system overview of the IC. Next, section III provides insights in the circuit topologies. Section IV provides measurement results after which conclusions are drawn in section V.

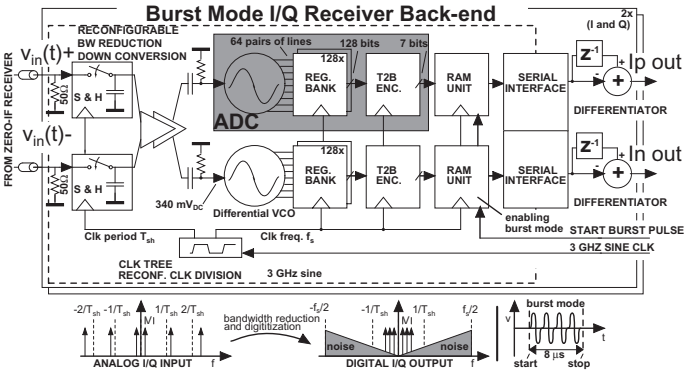

Fig. 1. The system topology. The S&H device provides a sampled, bandwidth-reduced, signal to two analog gain stages. Next, the resistor-capacitor network enables an ADC input biasing close to the lower supply rail. A dual ADC implementation digitizes the bandwidth-reduced signal. The VCO's phases are sampled, encoded and put in the SRAM-unit for burst mode operations. The dashed box highlights the IC content.

II. System Overview

The complete system is drawn in Fig. 1. It is designed to process, digitize and store the wideband I/Q decomposed analog output of a 60 GHz front-end. E.g. it is compatible with the output of a direct conversion receiver [8] (zero-IF). For illustration purposes, only one path of the quadrature decomposed processing hardware is shown. Due to the high power cost associated with a high baseband bandwidth, the signal is sub-sampled [9] by means of a sample-and-hold device (S&H), reducing its bandwidth. In certain applications, e.g. wireless positioning by time-of-arrival (ToA), this sub-sampling is beneficial. In this field, enabling a broad signal bandwidth B at the cost of a reduced SNR (due to the bandwidth reduction) provides better ToA estimation precisions than starting from this reduced bandwidth initially. The positioning performance bounds provided by [2], [10], [11] show this clear advantage of having this high received signal bandwidth B while keeping the product $B \cdot \mathrm{SNR}$ constant. The aliased, sub-sampled signals retain the same phase information as their high-frequent original and thus ToA can still be estimated based on the bandwidth reduction. In order to control the amount of bandwidth reduction, the S&H clock division is made reconfigurable. Apart from bandwidth reduction, the S&H could perform down conversion from an intermediate frequency for bandpass signals, as an alternative application.

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The sub-sampled signal is buffered to drive the big input capacitance of the connected VCO-based ADC topology (50 fF per VCO). Inside the ADC, the modulated VCO output is sampled and encoded into a binary representation after which it is fed to an on-chip SRAM data buffer, recording burst measurements. The resulting effect of the system on the signal is shown in the bottom part of Fig. 1. The ADC's quantization noise is shaped to high frequencies [4] whereas the multi-carrier signal is in the lower regions of the band. Since propagation losses in the EHF range are significant (more than 10 dB signal power loss when the distance doubles in the 60 GHz band), an effective resolution of 6 bits for both I and Q channels was the design goal for super-meter data communications and positioning applications.

The basic principle of the VCO-based ADC, as part of the system is shown in Fig. 2. The baseband input signal $v_{\rm in}(t)$ modulates the VCO by frequency modulation. The VCO's phases $\varphi_i(t)$ are periodically sampled after which the sampled thermometer encoded phases are thermometer-to-binary (T2B) encoded to $\Phi[k]$. Since the phase represents the integral of the input signal, a discrete-time differentiation is needed in order to obtain the digital signal ($v_{\rm out}[k]$). A high VCO-sample rate f_s enables low in-band noise due to the first order noise shaping associated with the topology.

The structure of Fig. 2 is implemented four times. This enables a differential implementation of both I and Q channels, reducing even order harmonics.

A. Sample and Hold Device

The bandwidth reducing S&H-operation also has implications on the precision of the digitization performed by the VCO-based ADC. Adding an S&H to the VCO-based topology is once performed in a theoretical work [5], shaping the noise in a bandpass way, increasing the precision. Here, a different precision-increasing effect is explained. Without an S&H device, the VCO's phases of the ADC would satisfy the following expression:

$$\varphi_i(t) = \sin\left(2\pi \int_0^t \left[f_0 + Dv_{\rm in}(\tau)\right] d\tau + \frac{2\pi \cdot i}{N}\right) + 1. \quad (1)$$

D is the VCO gain factor. $2N$ is the amount of VCO phases. f_0 is the VCO's free running frequency. After the sampling and differentiation of the VCO phases, $v_{\rm out}[k]$ equals [3]:

$$\begin{aligned} v_{\rm out}[k] &= \Phi[k] - \Phi[k-1] \quad (2)\\ &= [\![N\left(\int_0^{kT_s} f_0 + Dv_{\rm in}(\tau)d\tau - \int_0^{[k-1]T_s} f_0 + Dv_{\rm in}(\tau)d\tau\right)]\!] \\ &= \underbrace{NT_sDv_{\rm in}(kT_s)}_{\text{Wanted output}} + NT_sf_0 + {\rm Err}_{\rm int} + {\rm Err}_Q, \quad (3)\end{aligned}$$

with $T_s = 1/f_s$. $[\![\ ]\!]$ is the rounding operator, implementing the quantization. ${\rm Err}_{\rm int}$ and ${\rm Err}_Q$ are respectively the integration and quantization error terms. The latter is first order noise shaped. The S&H device (Fig. 2) will eliminate the ${\rm Err}_{\rm int}$ term in (3), enabling a more accurate digitization for high

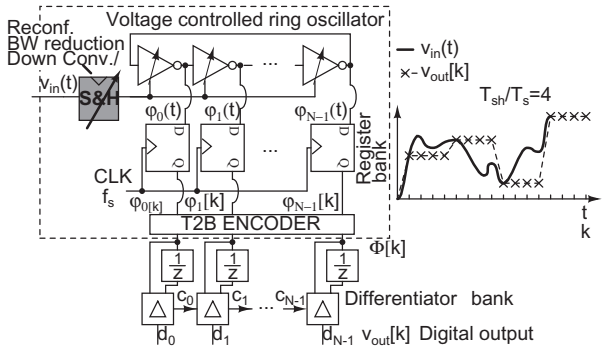

Fig. 2. Left: Core functionality of a VCO-based ADC, with an additional S&H. Right: Output of the VCO-based ADC for a sub-sampling of 4.

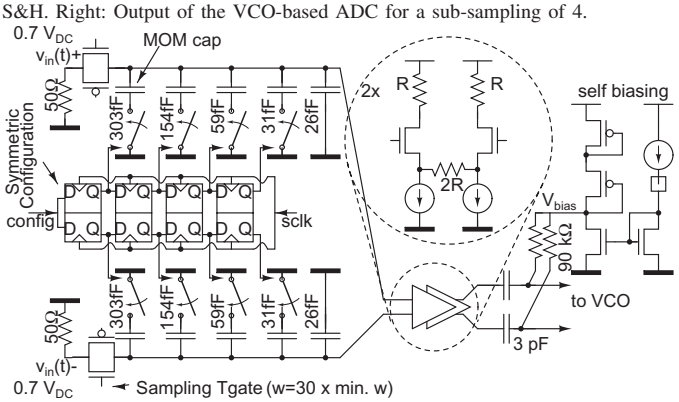

Fig. 3. Reconfigurable bandwidth reduction by means of S&H, analog buffer stages, and VCO input capacitive coupling. The configuration registers are implemented two-fold in order to preserve symmetry. The VCO input capacitive coupling is applied in order to steer the VCO input in its preferred voltage region of operation.

frequencies. This is seen as follows: an S&H will alter (1) into

$$\varphi_i[k] = [\![\sin\left(2\pi \sum_0^{kT_{\rm sh}} \left[f_0 + Dv_{\rm in}(kT_{\rm sh})\right] T_{\rm sh} + \frac{2\pi \cdot i}{N}\right) + 1]\!], \quad (4)$$

yielding for $v_{\rm out}[k]$ (based on (2)):

$$v_{\rm out}[k] = \underbrace{NT_{\rm sh}Dv_{\rm in}(kT_{\rm sh})}_{\text{Wanted output}} + NT_{\rm sh}f_0 + {\rm Err}_Q. \quad (5)$$

The S&H, sampling at a period of $T_{\rm sh}$, thus eliminates the ${\rm Err}_{\rm int}$ term. This is because the discrete differentiation which needs to be performed (Fig. 2) is now the perfect inverse of the integrating property of the VCO and its S&H. This states that the S&H is both interesting from a system point-of-view (the bandwidth reduction) and from a precision point-of-view (elimination of the integration error term). If the VCO itself is sampled at a high f_s, the first order noise shaping effect, inherent to the topology, becomes more pronounced [4].

The output contains a DC-offset of $NT_{\rm sh}f_0$ which can be ignored since a multi-carrier allocation generally does not foresee a carrier at DC.

B. SRAM Data buffer

The VCO sample rate is $f_s = 3\,{\rm GH}z$. Due to the high output bit rate of the I/Q digitizers (96 Gb/s), on-chip data

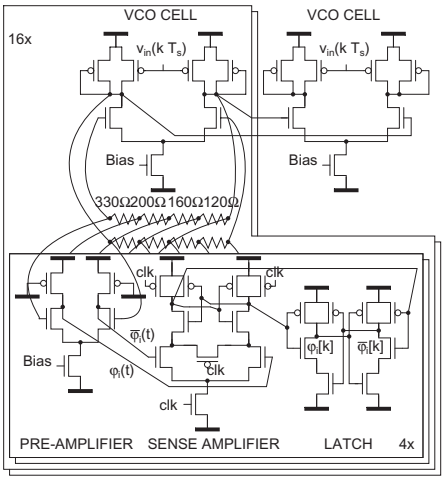

Fig. 4. The VCO-topology, its pre-amplification, strobed sense-amplification and latch circuits. The pre-amplification prevents kick-back from the sampling clock.

buffering is applied. This facilitates the data transfer to the host which does not have to be high-speed capable. The IC has a recording window of $8\,\mu$s. This $8\,\mu$s is enough to store a complete digitized multi-carrier positioning or data communications signal. Four single-port 32 bit SRAM ip-cores, addressable by a 13 bit address word compose the buffer. A custom serial controller is integrated in order to clock the data serially out of the core to the host IC.

III. Circuit Topology

Fig. 3 shows the analog bandwidth-reducing circuitry. In order to achieve a high input bandwidth, the sampling device is a single transmission gate, performing parallel sampling [12]. The less area-optimized but linear behavior of rotational MOM-devices is chosen as a capacitor technology. Capacitors can be switched on and off at run-time, implementing the trade-off between bandwidth and hold-time. This is a useful option whenever the system's bandwidth is reduced when a reduced positioning precision or data communications bit rate is needed.

The sampling clock can be reconfigured in order to implement the sub-sampling operation. The amount of sub-sampling is defined as the ratio T_{sh}/T_s. The S&H clock can be divided from the master clock up to a value of 128. After the S&H operation, the signal is buffered by means of a high-impedance input cascade of two source degenerated unity-gain buffers. The source degeneration provides additional linearity. Finally, the signal is AC-coupled to the VCO input. This is in order to enable the VCO and the buffers to work in its preferred biasing conditions to maximize its linearity, which is $340\,\mathrm{mV_{DC}}$. Additionally, possible DC-shifts due to LO-feedthrough in direct conversion receivers are not applied to the VCO. Since this is close to the lower supply rail of $0\,\mathrm{V}$, achieving this by active devices will decrease the linearity. The inherent zero-frequency of the AC-coupling of $0.6\,\mathrm{MHz}$ is affordable as long as the discrete multi-carrier spectrum does not foresee a sub-carrier that close to DC, which is the case for most applications.

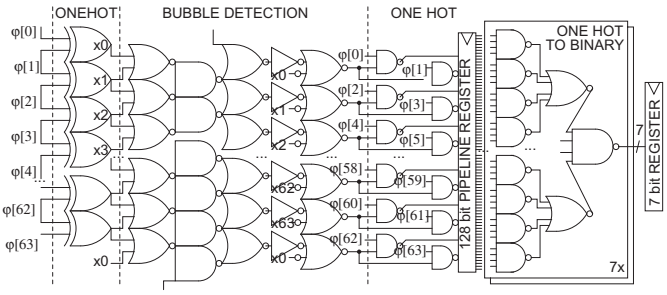

Fig. 5. The T2B encoder. A bubble detection of depth 4 is applied in order to deal with VCO-phase non-linearities. Due to the depth of the combinatoric path, a pipeline stage is added, relaxing setup-time violation requirements.

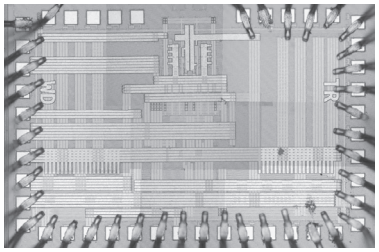

Fig. 6. 44-pin die micrograph of the $40\,\mathrm{nm}$ IC realization.

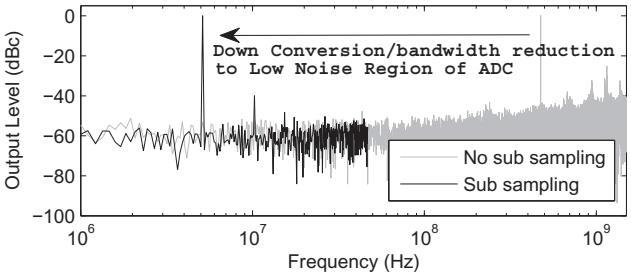

Fig. 7. IC output when applying a tone at $474\,\mathrm{MHz}$. Input power is $-4\,\mathrm{dBm}$. Disabled sub-sampling ($T_{\mathrm{sh}}/T_s = 1$) doesn't exploit the advantage of the first order noise shaping property. Whereas enabled sub-sampling ($T_{\mathrm{sh}}/T_s = 32$) provides a good digitization.

Fig. 4 shows a circuit-level drawing of the core VCO delay cell and its sampling. The upper half of the figure shows the biased VCO cell. Its structure is introduced in [13]. Thanks to the diode-connected pmos load, the input differential of the VCO tends to stay in its saturation region, providing a speed advantage with respect to full swing digital VCO cells. The VCO cell outputs are 4-times interpolated by resistors in this design. The 4 resistor values are non-identical in order to provide equidistant time-domain interpolation. After interpolation, the VCO-signal is pre-amplified in order to prevent the clock from introducing kick-back in the VCO. The pre-amplifier mosfet sizings are the same as those of the VCO cell, making reuse of its biasing voltage possible. A sense-amplifier and latch represent the boundaries between the analog and digital domain.

Fig. 5 shows the T2B encoder. In order to catch the effects of non-linearities and noise in the thermometer-encoded phases $\varphi_i[k]$, a bubble detection of depth 4 is implemented.

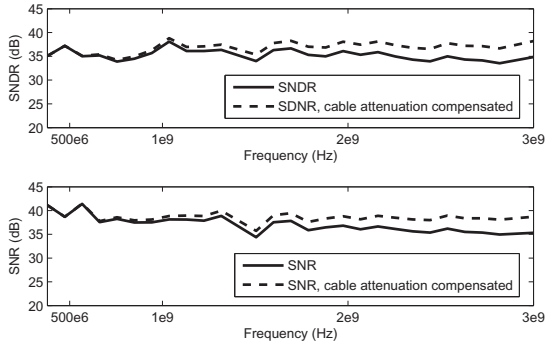

Fig. 8. SNDR and SNR as a function of the input frequency for $T_{\rm sh}/T_s = 32$ and $f_s = 3\,\mathrm{GHz}$. Additionally, cable attenuation is compensated based on measurement data. The bandwidth is defined up to the aliased third harmonic component. The input power equals $-4\,\mathrm{dBm}$.

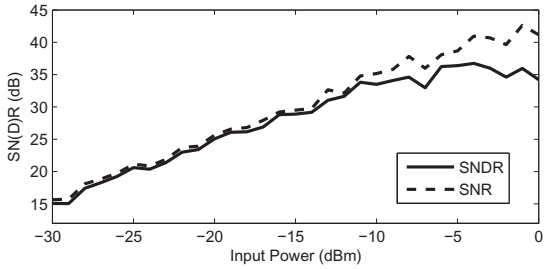

Fig. 9. SNDR and SNR as a function of the input power. The input frequency is $474\,\mathrm{MHz}$. $T_{\rm sh}/T_s = 32$ and $f_s = 3\,\mathrm{GHz}$.

IV. Measurement Results

The design is processed in a $40\,\mathrm{nm}$ general purpose CMOS technology. Apart from the SRAM ip-blocks, the complete layout is full custom. Fig. 6 shows the $1.6\,\mathrm{mm}^2$ IC realization. The core (no SRAM and I/O) occupies $0.162\,\mathrm{mm}^2$.

The IC is measured at a sample rate of $f_s = 3\,\mathrm{GHz}$. The $-3\,\mathrm{dB}$ input bandwidth is measured at $3\,\mathrm{GHz}$ in a setup where attenuation effects of wire delays are compensated. Fig. 7 shows the DFT power spectrum of a $474\,\mathrm{MHz}$ input both when the S&H sub-sampling is enabled and disabled. The applied differential input power is $-4\,\mathrm{dBm}$ ($560\,\mathrm{mV_{pp}}$). Sub-sampling improves the $\mathrm{SN(D)R}$ by shifting the signal peak to a low noise region in the spectrum. The spurious-free-dynamic-range (SFDR) is $40\,\mathrm{dB}$ based on the graph. The $\mathrm{SN(D)R}$ figures as a function of input frequency for an input power of $-4\,\mathrm{dBm}$ and sub-sampling are shown in Fig. 8. No static linearity post-calibration is performed to boost up the performance. At an input frequency of $3\,\mathrm{GHz}$, the SNDR is $38\,\mathrm{dB}$ yielding $6\,\mathrm{effective\ bits}$ (ENOB). Fig. 9 illustrates the dynamic range of the converter. Optimal SNDR conditions are found for an input power range of about $-10\,\mathrm{dBm}$ — $0\,\mathrm{dBm}$. Power consumption for a single core is measured to be $58\,\mathrm{mW}$. This excludes I/O and SRAM buffer overheads. Table I compares this design to the state-of-the-art of open loop VCO-based ADC topologies. Due to the new sub-sampling, the bandwidth is extended to the GHz-range. The VCO-sample rate is the highest, yielding the highest Nyquist bandwidth ($1.5\,\mathrm{GHz}$) when sub-sampling is disabled.

TABLE I
Comparison Table

	This	[4]	[6]	[7]
Analog. Inp. BW.	3 GHz (6 GHz I/Q)	100 MHz	500 kHz*	20 MHz
Sampling clock	93.5 MHz‡	500 MHz	10 MHz*	600 MHz
Power/Core (-MEM -I/O)	58 mW	12.6 mW	475 μW*	14.3 mW
Tot. power (+MEM +I/O)	233 mW			
Number of Cores	2 (I/Q)	1	1	1
Area (-MEM -I/O)	0.162 mm²§	0.078 mm²	N/A	0.12 mm²
SNDR	38 dB	36.7 dB**	56 dB*	52.5 dB
CMOS Tech.	40 nm	130 nm	180 nm	130 nm
Nominal Supply	0.9 V	1.2 V	1.8 V	N/A
S&H Sub-sampling	YES	NO	NO	NO
I/Q BB. 60 GHz enabled	YES	NO	NO	NO
Burst Buffering	48 kB	N/A	N/A	N/A

∗ based on simulations ‡ sub-sampling of 32: $f_s/32$
§ area of **I/Q** VCO ADC Core ** linearity calibration

V. Conclusions

This paper introduced a $6\,\mathrm{GHz}$ RF bandwidth I/Q receiver back-end for $60\,\mathrm{GHz}$ discrete carrier applications. The bandwidth-reducing operation on the discrete spectrum enables using a VCO-based ADC topology, exploiting the linear noise shaping behavior of the topology at its maximum. This achieves an accurate digitization of 6 effective bits even for high frequency carriers up to $3\,\mathrm{GHz}$. Due to the high sample rate of $3\,\mathrm{GHz}$ and supporting burst-mode operation, on-chip data buffering is applied. Power is measured at $106\,\mathrm{mW}$ for both cores.

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